4k x 2k and 4k x 4k CCD Users Manual

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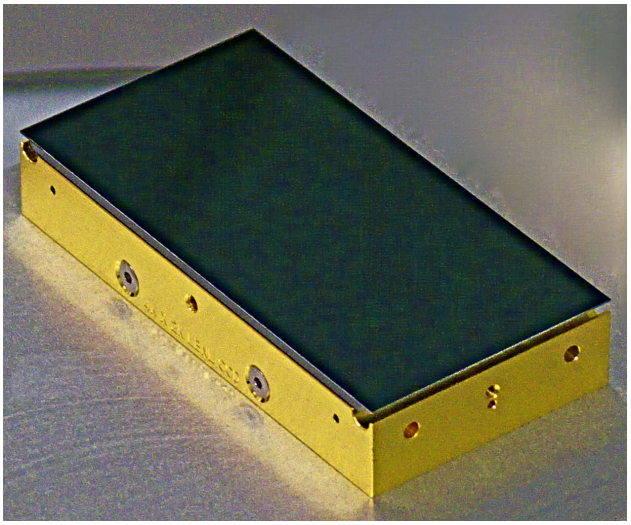


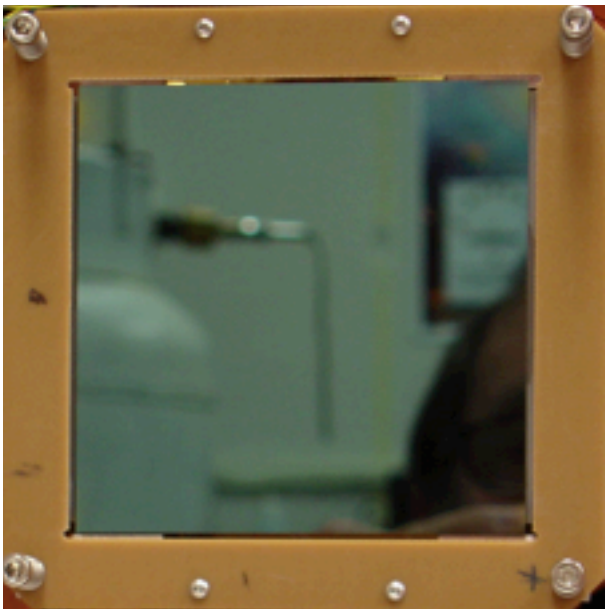


Table of Contents

1 CCD description

1.1 Introduction

The LBNL 4k x 4k and 4k x 2k CCDs are 250 μm thick, fully depleted p–channel devices with 15 μm pixels. Both formats are available in a buttable package with an invar base and a single flex-circuit with a 65-pin nano-style connector, and in a window-frame style PCB package with two 37-pin nano-style connectors.

1.2 Performance

The quantum efficiency (QE) of the LBNL fully depleted CCDs is outstanding in the near infrared (NIR), up to about 1000 nm. The NIR QE depends on the thickness of the fully depleted sensitive region (improving with thickness) and on the operating temperature (improving as temperature is increased due to phonon assisted tunneling). We show a typical QE curve in **Figure 1**. Other performance parameters are summarized in **Table 1**.

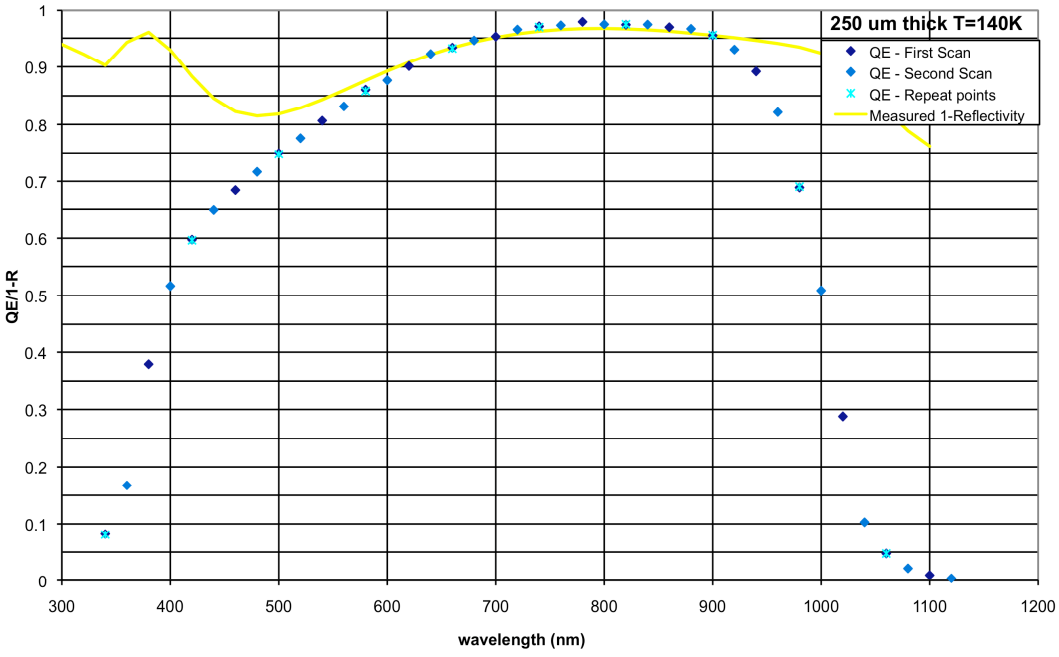
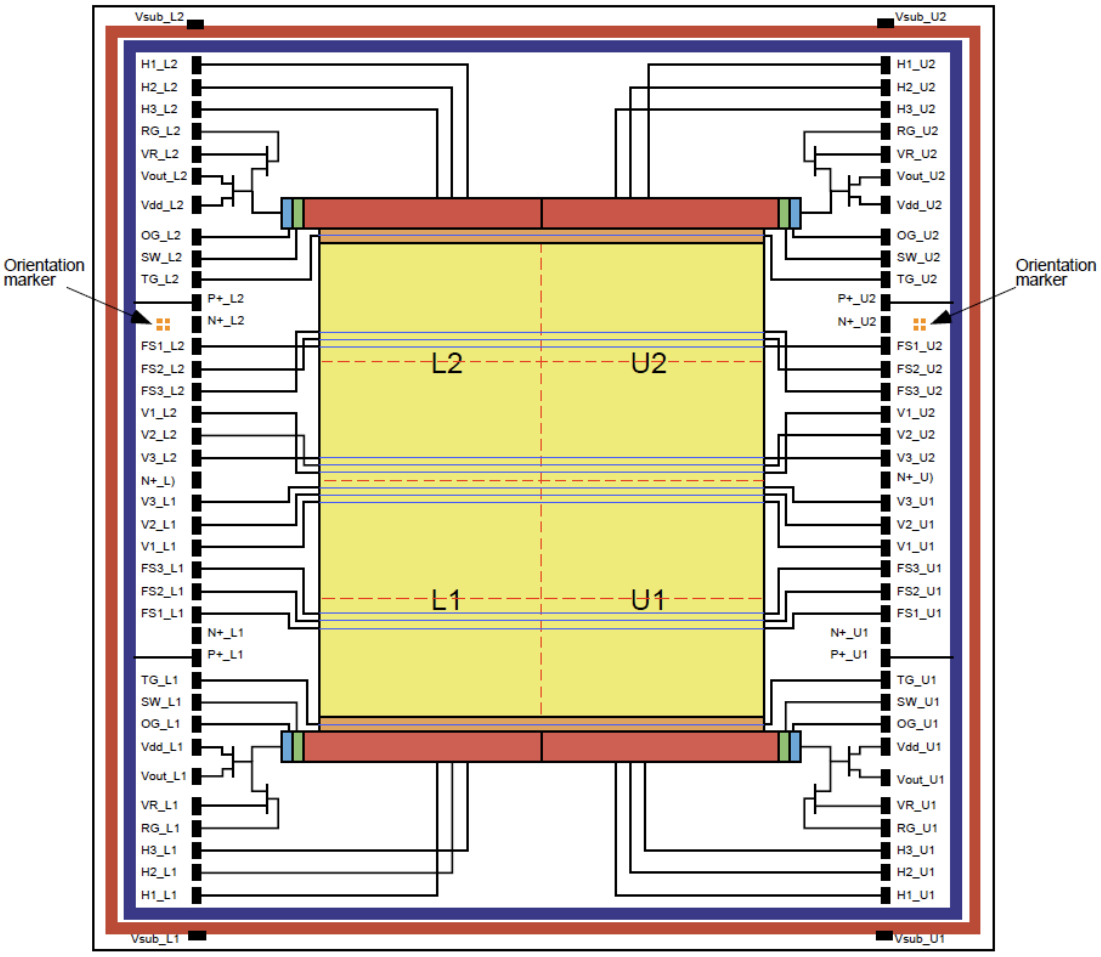


Figure 1 Quantum efficiency versus wavelength (blue points) and 1-reflectivity (yellow line) for a 250 um thick LBNL CCD measured at 140K. The QE should be very close to 1-R in the central wavelength region. Surface absorption dominates for wavelengths below 500 nm, and silicon becomes increasingly transparent to light above 900 nm due to the increasing absorption length.

Table 1

Parameter	Units	Typical Value	Comment
Read Noise	electrons	3	70 kHz
CTE		>0.99999	serial and parallel
Dark Current	e-/pix/hour	<5	for T<170K
Flatness	microns	+/- 10	peak to valley



Frontside view

Figure 2 A cartoon showing the CCD layout, pad labels and quadrant numbering. The orientation marker is printed on the CCD die on the U2/L2 side.

2 Signal naming convention

1. The CCD is divided into two halves labeled 1 and 2 along the pixel columns. Each half has its own serial register.
2. Half 1 and 2 are further divided into U and L, so the CCD readout quadrants are labeled U1, U2, L1, and L2.
3. Serial and parallel clock phases are labeled 1, 2, and 3.
4. Labeling: p=1, 2, or 3 for clock phases; c=1 or 2 to denote halves; h=U or L to denote the two serial readout sectors on each half.

3 Signal descriptions

3.1 Parallel clocks

3.1.1 Vp_c

1. Parallel register clocks (a.k.a., vertical clocks) for pixel rows farthest from serial register.
2. The three phases have identical voltage swings.
3. Vertical clocks from the U and L sides are bussed together within the CCD.

3.1.2 FSp_c

1. Parallel register clocks (a.k.a., vertical clocks) for pixel rows closest to serial register.
2. The three phases have identical voltage swings.
3. Vertical clocks from the U and L sides are bussed together within the CCD.

3.1.3 TG_c

1. Parallel register to serial register transfer gate clocks.
2. Side 1 and 2 clocks have identical voltage swings.
3. Transfer gate clocks on U and L sides are bussed together within the CCD.

3.2 Serial clocks

3.2.1 Hn_hc

1. Serial clocks for four quadrants of serial readout register (a.k.a., horizontal clocks).
2. The three phases have identical voltage swings.

3.2.2 SW_hc

1. Serial register to summing well transfer clock.
2. The four instances are independently controlled.

3.2.3 RG_hc

1. Floating diffusion capacitor reset gate clock.
2. The four instances are independently controlled.

3.3 Bias voltages

3.3.1 OG_hc

1. Summing well / floating diffusion isolation gate (DC).

3.3.2 VR_hc

1. Floating diffusion capacitor reset reference voltage (DC)
2. The four instances are independently controlled.

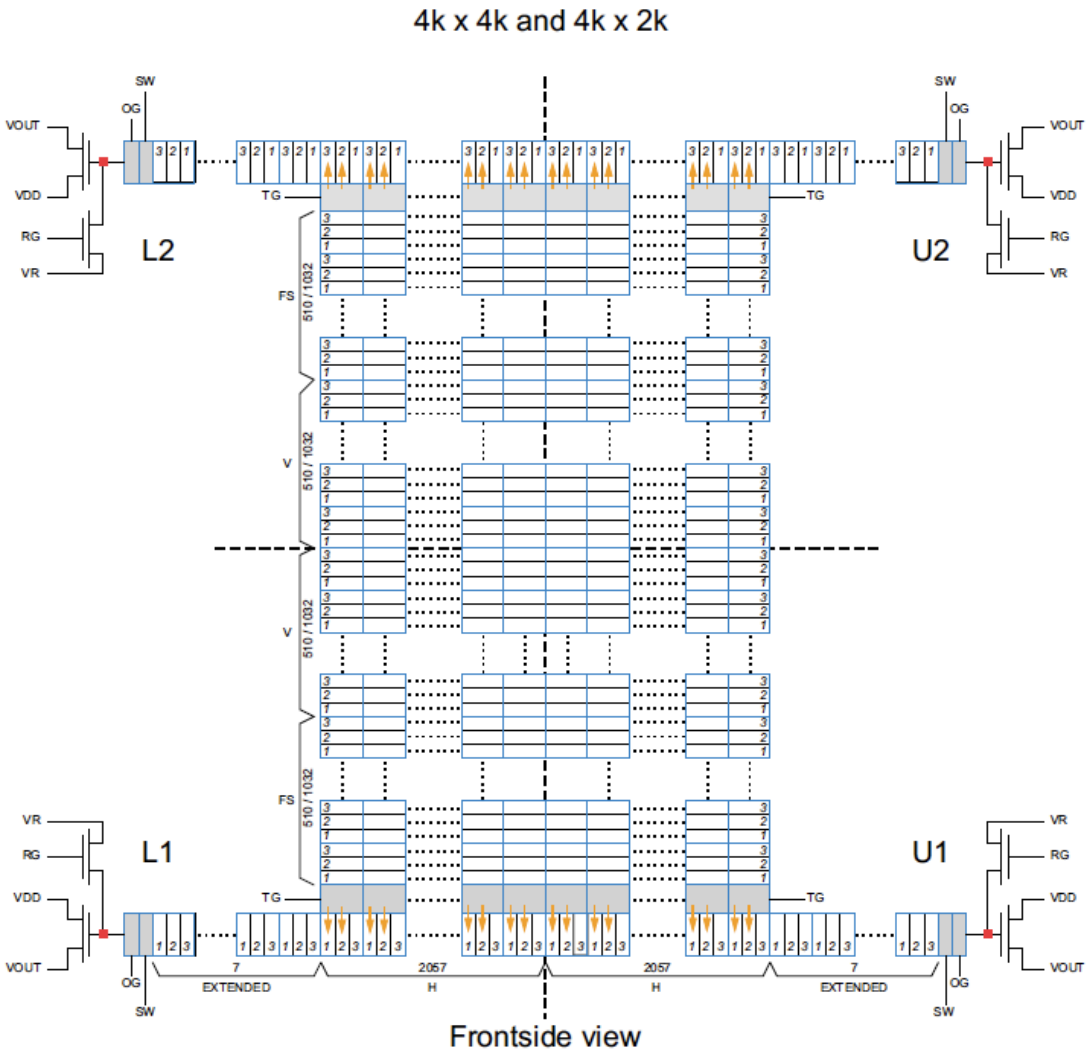


Figure 3 A diagram showing the clock phase ordering. Note the device is diagonally symmetric. Both serial and parallel channels are continuous and can be read at either or both ends. There are 7 extended pixels.

3.3.3 VDD_hc

1. Readout source follower transistors drain voltage (DC).
2. Recommend external >15 μF, 35V capacitor to P+.

3.3.4 VOUT_hc

1. Readout source follower transistors sources – output signal.
2. Recommend 20-30 kΩ load resistor to P+ (included in buttable package)
3. Recommend 1 μF, 50V capacitor in series to external signal processing.

3.3.5 P+

1. p+ guard ring contact (DC).
2. Four instances are bussed together within the CCD.
3. By convention, this node is 0V; all other voltages are referenced to this.

3.3.6 N+

1. n+ channel stop implant contacts.
2. All N+ contacts are bussed together within the CCD.
3. Recommend 100 nF, 200V capacitor in parallel with 4MΩ resistor to P+ (included in buttable package).

3.3.7 VSUB

1. Substrate depletion voltage (DC).
2. All VSUB contacts are bussed together within the CCD.
3. Recommend 1000 nF, 200V capacitor to P+.
4. Nominal operating voltage is +40V to +80V; full depletion is typically achieved around 20V depending on substrate resistivity. Devices may be operable up to 100V or more.

4 Signal AC and DC requirements

Table 2 lists the nominal operating voltages for the CCD in its different modes of operation and recommended maximum voltage ranges. Also given are recommended rise-fall times for operation at typical readout rates (100 kpix/sec). Table 3 lists the approximate capacitances between various clock lines.

Table 2

Signal	# of copies	Type	Exposure VL	Exposure VH	Readout VL	Readout VH	Erase VL	Erase VH	Purge VL	Purge VH	Adj. Range VL	Adj. Range VH	t width (µsec)	I
V1	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	
V2	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	
V3	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	
FS1	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	
FS2	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	
FS3	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	
TG	2	ck	-3	5	-3	5	-4	6	-4	6	-5	10	50	
H1	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5	
H2	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5	
H3	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5	
SW	4	ck	-5	5	-5	5	-5	5	-5	5	-8	8	0.5	
RG	4	ck	-6	0	-6	0	-6	0	-6	-6	-8	0	0.15	
OG	4	dc	2.2		2.2		2.2		2.2		0	5		
VR	4	dc	-12.5		-12.5		-12.5		-12.5		-15	0		
VDD	4	dc	-22		-22		-22		-22		-25	0		<1 mA
VOUT	4	ac												
VSUB	1	dc	+40 to +80		+40 to +80		0		0		0	100		<1 µA
N+	3	float												
P+	1	dc	0		0		0		0		0			

Table 3

Signal	4kx4k Cap 1032 lines	4kx2k Cap 510 lines	
V1 to V2-V3 (typ)	85	42	nF
FS1 to FS2-FS3 (typ)	85	42	nF
FS3-TG	300	300	pF
H1 to H2-F3 (typ)	180	180	pF
SW	small	small	pF
RG	small	small	pF

5 Sensitivity and source follower noise

The sensitivity of the output stage is ~3 μV/e for I_{ds}= 600 μA and V_{ds}=5V. The noise voltage spectrum is shown in Figure 4 for i_{DS}=600 μA and V_{ds}=5 V. A good approximation is 1 µV at 1 Hz for 1/*f* noise and 15 nV/√Hz for white noise. The output impedance is approximately 4 kΩ.

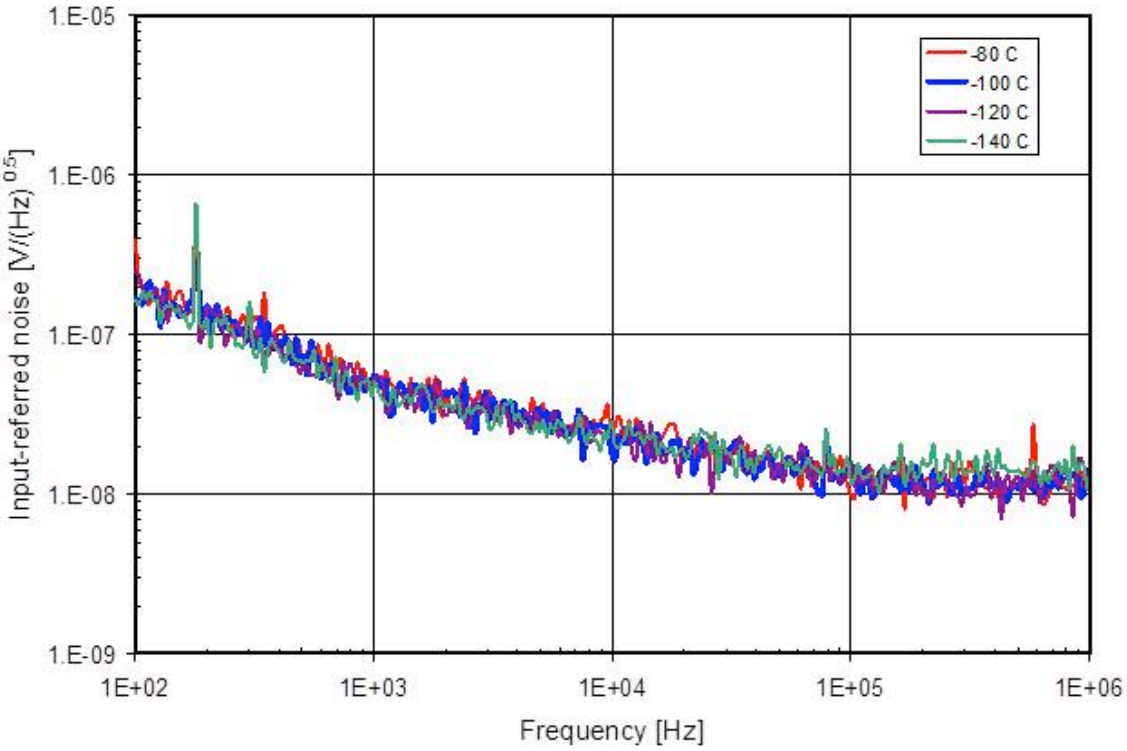


Figure 4 Input referred noise versus frequency for the output transistor measured at four different temperatures.

6 Binning

The serial register can accommodate charge from three binned parallel pixels. The summing well can accommodate charge from three binned serial pixels, or up to nine unbinned parallel pixels.

7 Clocking

7.1 Parallel clocking

Figure 5 shows a parallel clocking sequence. Charge accumulation occurs in the low voltage phase of the gates because the p-channel collects holes instead of electrons.

7.2 Serial clocking

Figure 6 shows a serial clocking sequence, including reset gate and summing well operation.

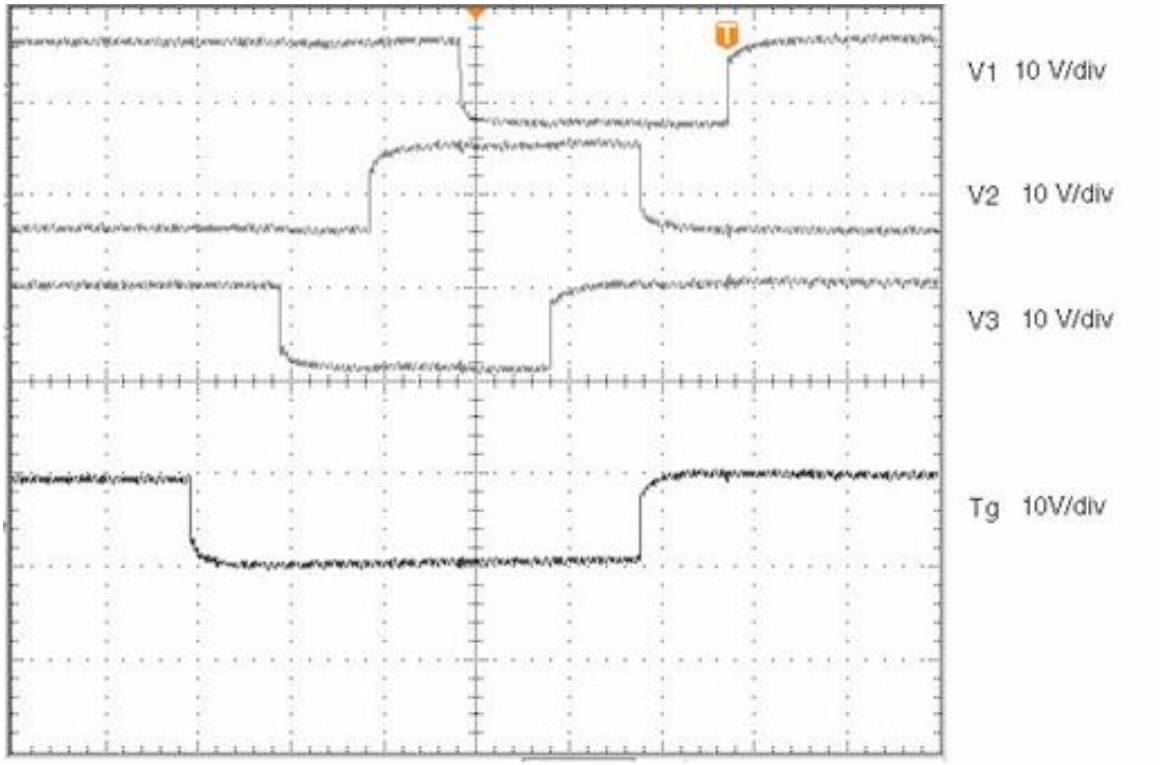


Figure 5 Example clocking sequence for the vertical clocks, including transfer gate.

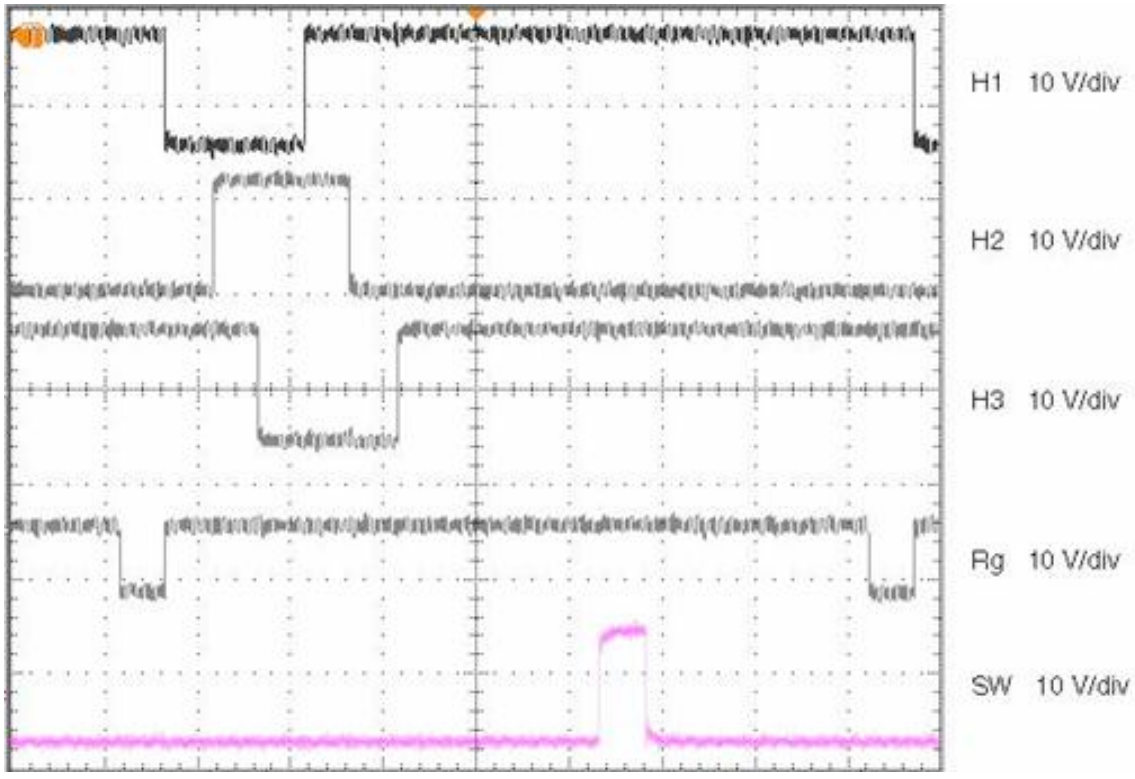


Figure 6 Example of serial clocking sequence, including reset gate and summing well.

8 Modes of operation

8.1 Serial clocking

Figure 7 shows that the serial register can be read in one of three ways, split read, read left, and read right. Split read is the nominal mode since this minimizes the overall readout time.

There is a fourth mode where all the serial clock phases and summing well are held low so that the serial register is a simple conducting channel, with the reset gate kept on to dump charge. This is used for erase and purge modes as described below, and for idle mode in which the parallel clocks are continuously running to flush charge out of the imaging region.

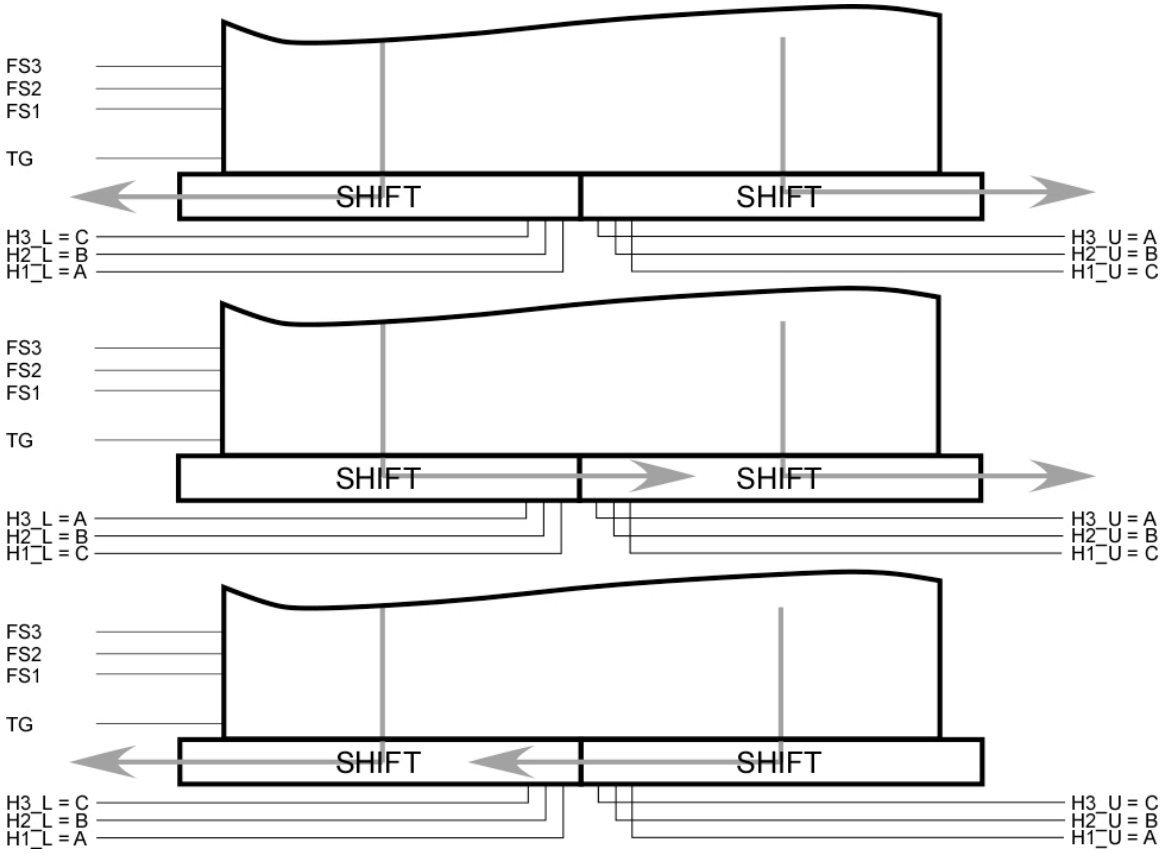


Figure 7 Serial register operation for split read or readout through the right or left transistors. A, B and C denote the ordering of the three phase clock operation.

8.2 Standard four-corner read out of entire CCD

Figure 8 shows readout of the entire CCD. The corresponding clock pairs of V1-3 and FS1-3 are clocked identically, TG broadside loads the serial register, and each row of pixels is read out in split serial mode.

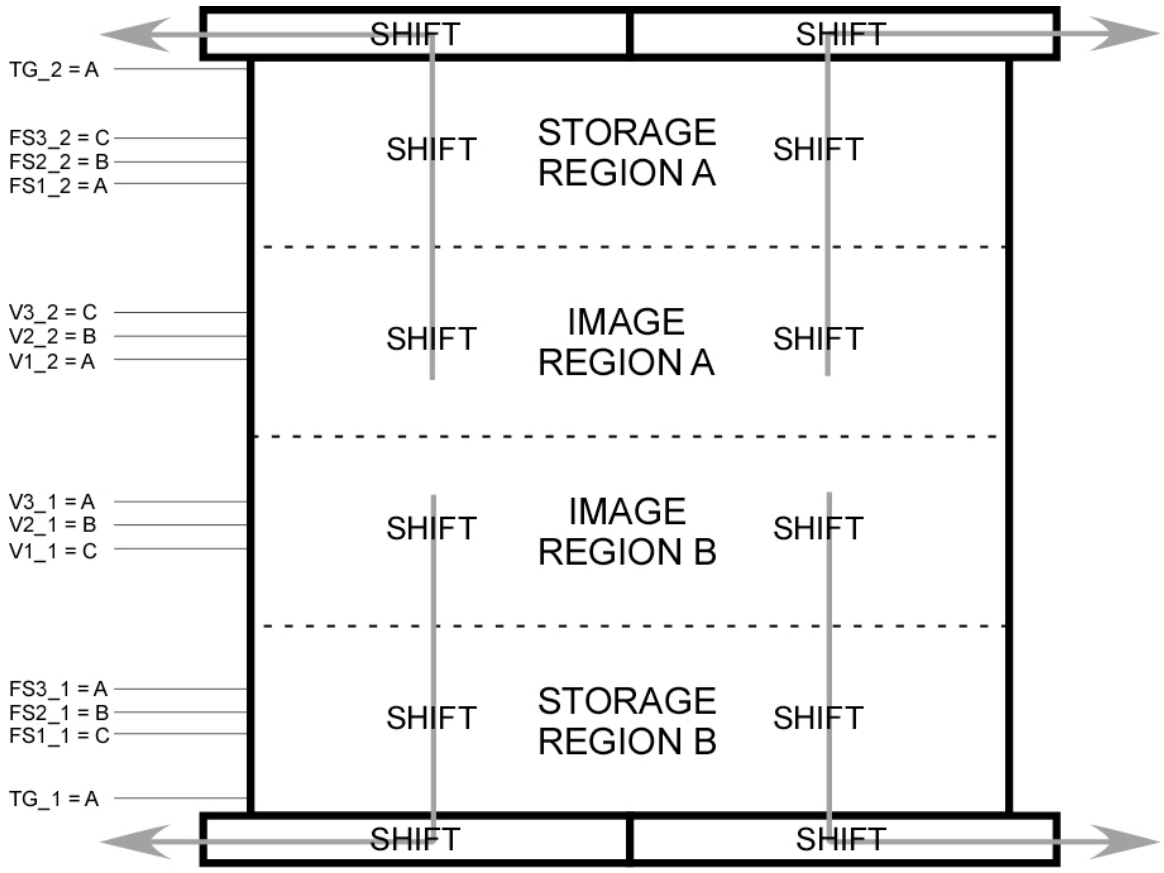


Figure 8 Standard clocking configuration to read out the entire CCD through four outputs. A, B and C denote the ordering of the three phase clock operation.

8.3 Readout of storage region only

Figure 9 illustrates readout of the storage region only. V1-3 are static and FS1-3 are clocked, while TG loads the serial register for split read.

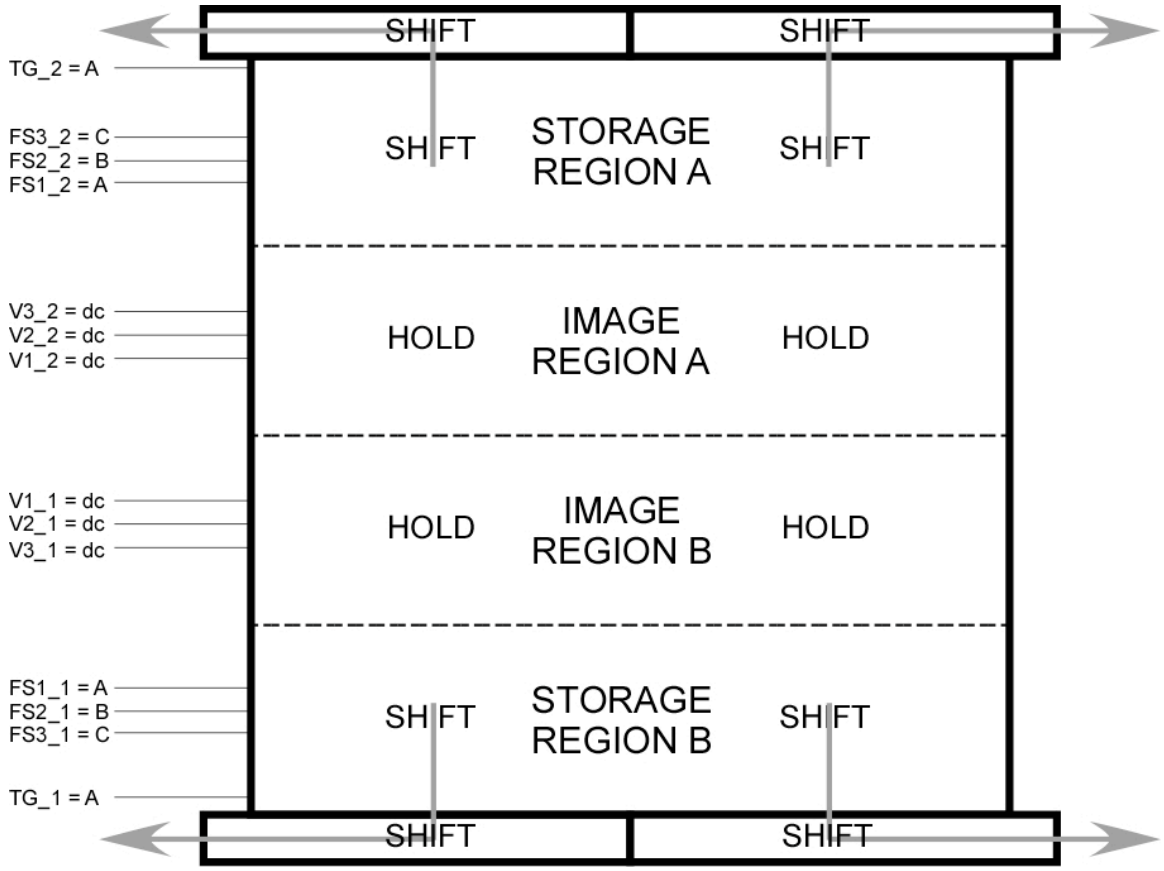


Figure 9 Readout of the storage region only using the frame store clocks while holding the central vertical clocks static. A, B and C denote the ordering of the three phase clocks.

9 Procedures unique to LBNL CCDs

9.1 Erase Procedure

When CCDs are first turned on or subjected to strong, saturating illumination, residual “ghost” images or high dark current signals may be produced. These are caused by the emptying of electron traps at the Si/SiO2 interface by the excess hole carriers produced by saturation. At low temperatures these traps refill slowly, releasing holes into the wells in a process extending over many hours.

These artifacts can be eliminated by an erase procedure that quickly re-populates the traps with electrons. The recommended procedure is as follows: ramp Vsub to 0 V in a controlled, linear manner and increase all parallel clocks to 10 V; this causes inversion and floods the surface with electrons. We use a linear ramp rate of about 75 V/s but a faster ramp is possible. After a brief delay (fraction of a second) ramp Vsub back to normal operating voltage. When Vsub > ~10 V restore the parallel clocks to normal values. Figure 10 shows an example waveform and parallel clocking sequence generated during an erase.

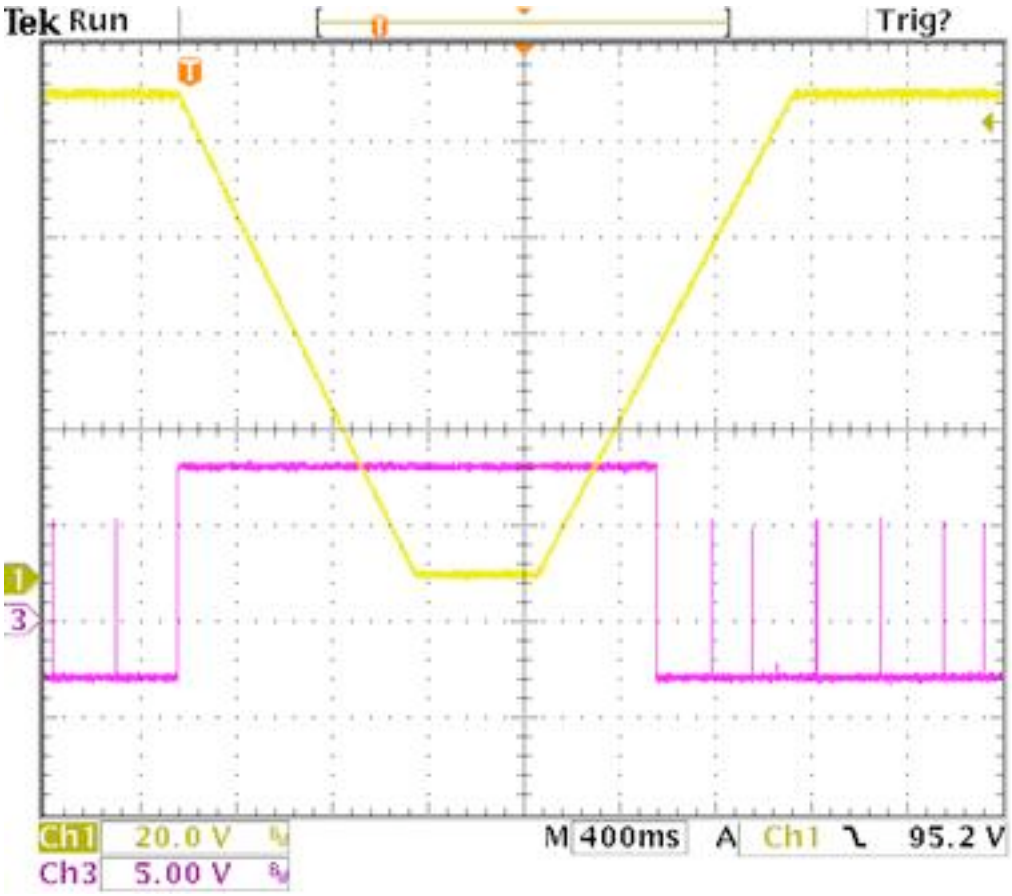


Figure 10 Erase procedure. The upper trace is Vsub and the lower trace is a vertical clock.

9.2 E-Purge Procedure

In the 4k x 4k and 4k x 2k CCDs, the individual channel stops become isolated electrically as Vsub is increased and it is possible for the channel stops to be left in different charged states after the initial low temperature power-up or after the erase procedure. The result is that images may have irregular baselines and a fixed pattern appearance in some regions.

This situation can be rectified by the following “e-purge” procedure: During the idle-mode prior to acquisition of an image, set all the parallel clocks to a strong

accumulation potential of -9 V and hold them there for a fraction of a second before restoring normal operation. During this procedure do NOT ramp or change Vsub. Once this procedure is completed, multiple clean, low-noise images can be acquired without further erase or e-purge procedures.

10 Precautions

10.1 ESD

LBNL CCDs are sensitive to electro-static discharge (ESD) and can be irreversibly damaged if ESD precautions are not taken. Proper ESD precautions include grounding the operator through a wrist strap, using static dissipative tools and mats, and handling devices only in a humidity controlled room (RH > 33%). The provided shorting plugs should be installed whenever the device is not connected to the readout electronics. When connecting the CCD to the readout electronics, the potential of the grounding plug should be equalized with the ground shield of the output connector prior to insertion.

10.2 Super-Saturation

The CCDs should not be subjected to excessively bright illumination while under static power. It is possible to damage the oxide layers under strong flat field illumination if the CCD is powered and the pixels are allowed to accumulate >1000 times the full well charge over a sustained period. If the CCD will be subjected to strong light it should be powered down. Exposure to ambient light for limited periods of time while powered is safe if the CCD is kept in idle mode, where the parallel clocks are running continuously and draining all charge into the serial register with all phases low, the summing well in accumulation mode and the reset transistor on.

10.3 Thermal operation

The CCD should be cooled and warmed at a controlled rate that should not exceed ~5 deg C per minute to avoid excess thermal stress. Nominal operating temperature is 140° – 170° K.

11 CCD Packaging

11.1 Buttable Package

The 4k x 2k CCD is available in a four-side buttable package format with a single 65-pin flex connector and an invar base. (A similar package for the 4k x 4k CCD is under development.) There are four JFET source follower transistors mounted on the flex circuit with their resistive loads, in addition to the recommended parallel resistor and capacitor between n+ and p+ and a PT1000 resistor that is glued to the silicon substrate for temperature monitoring. A photo showing the invar mount, flex circuit and JFETs is shown in Figure 11. The schematic is given in Figure 12.

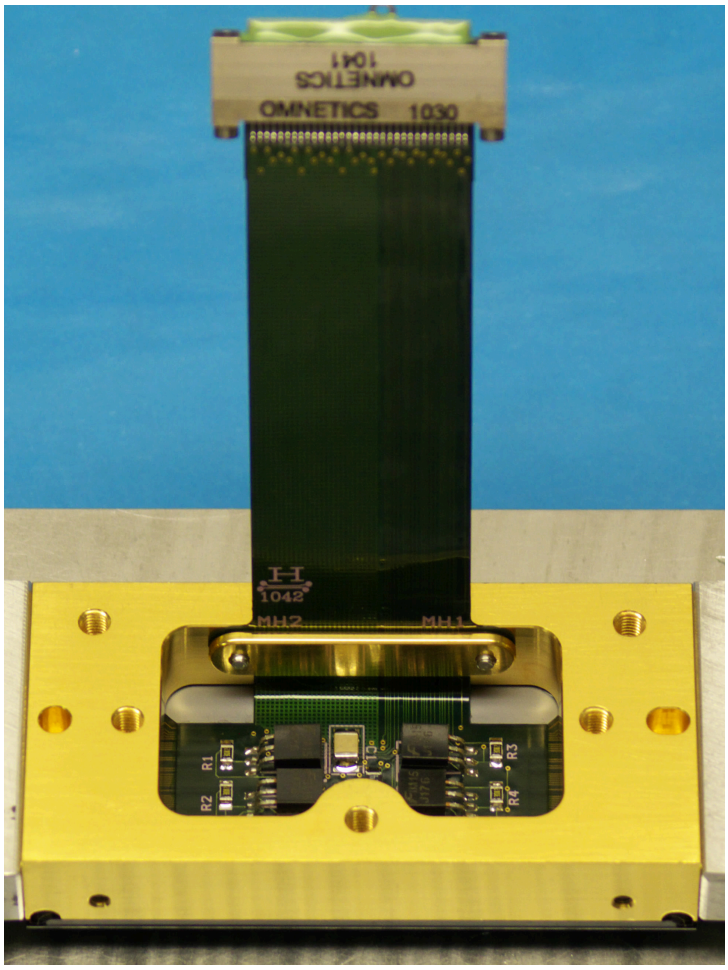


Figure 11 Photograph of the invar mount and flex circuit on the buttable 4k x 2k CCD. The four JFET source follower transistors and the RC circuit between p+ and n+ are also visible.

The package dimensions are 64.56 mm x 32.87 mm for the 4k x 2k CCD. The height of the packages is 11.58 +/- 0.02 mm. A drawing showing the locations of the mounting hole/slot and tapped screws in the invar mounting base is shown in Figure 13.

The buttable package has a single nano-miniature Omnetics connector A28300-065 (model# MNPO65FFNEJS); the pinout is given in Table 4.

Table 4

1	H1(U1)	34	H1(U2)
2	H1(L2)	35	H1(L1)
3	H2(U1)	36	H2(US)
4	H2(L2)	37	H2(L1)
5	H3(U1)	38	H3(U2)
6	H3(L2)	39	H3(L1)
7	SW(U1)	40	SW(U2)
8	SW(L2)	41	SW(L1)
9	RG(U1)	42	RG(U2)
10	RG(L2)	43	RG(L1)
11	V3(1)	44	V1(2)
12	FS3(1)	45	FS1(2)
13	V2(1)	46	V2(2)
14	FS2(1)	47	FS2(2)
15	V1(1)	48	V3(2)
16	FS1(1)	49	FS3(2)
17	TG(1)	50	TG(2)
18	TMP1	51	TMP2
19	P+	52	P+
20	VR(U1)	53	OG(U1)
21	VDD(U1)	54	VOUT(U1)
22	RL(U1)	55	RL(U1)
23	VR(U2)	56	OG(U2)
24	VDD(U2)	57	VOUT(U2)
25	RL(U2)	58	RL(U2)
26	VR(L2)	59	OG(L2)
27	VDD(L2)	60	VOUT(L2)
28	RL(L2)	61	RL(L2)
29	VR(L1)	62	OG(L1)
30	VDD(L1)	63	VOUT(L1)
31	RL(L1)	64	RL(L1)
32	P+	65	VSUB

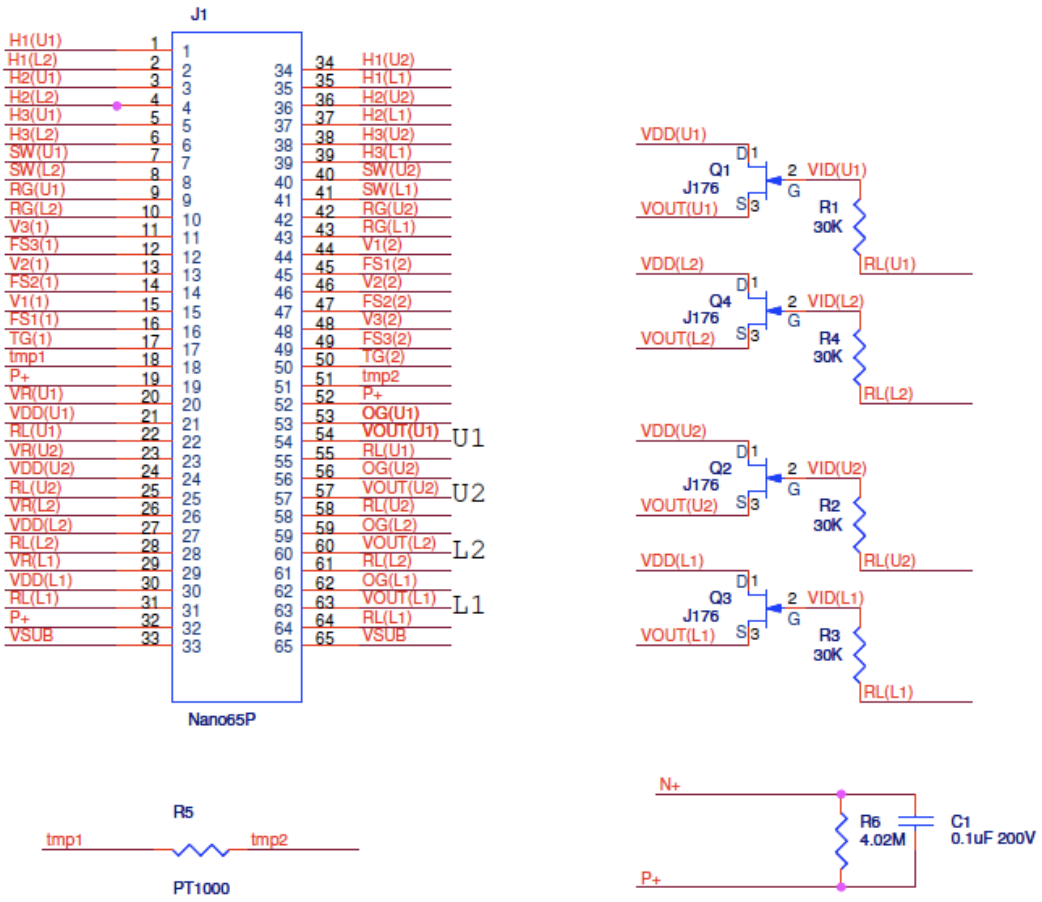


Figure 12 Schematic for the buttable package including the 65-pin connector pinout and the discrete components mounted on the flex circuit. VID is the internal video signal from the CCD to the gate of the JFET source follower. RL is the resistive load ground that provides the references for each corresponding VOUT signal and should be tied to ground at the input to the pre-ampflier.

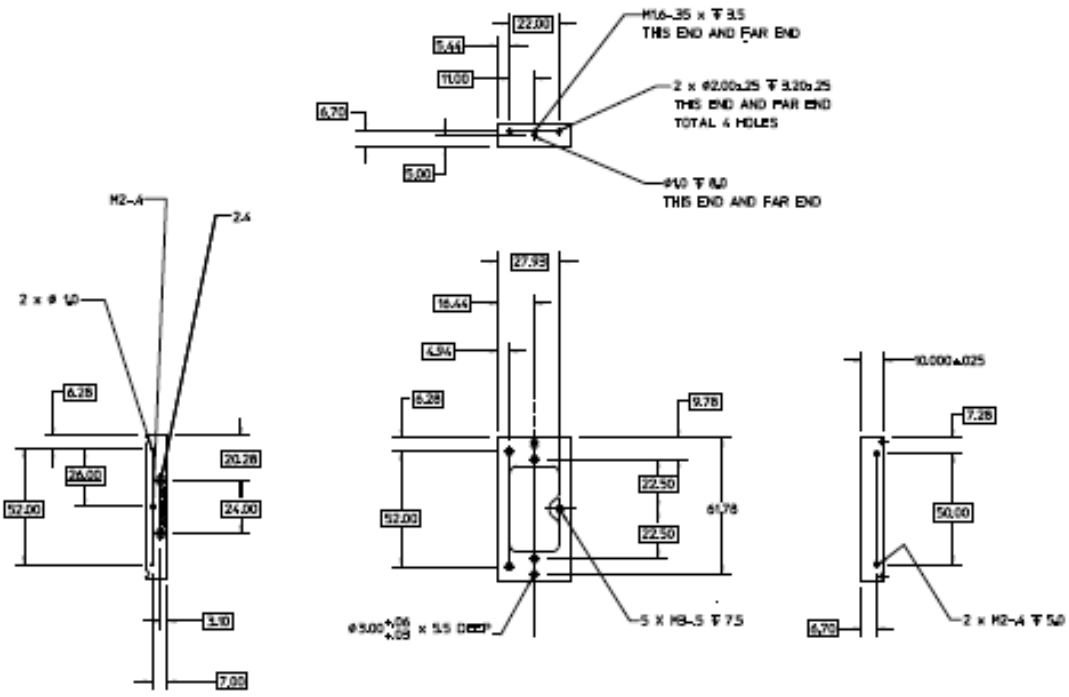


Figure 13 Drawing of invar base plate for the 4k x 2k buttable CCD package showing dimensions and locations of mounting hole/slot as well as tapped holes on the bottom for cooling straps and side holes device manipulation and for attaching a filter frame (not included).

11.2 Window frame package

For applications requiring a single CCD, a simple window-frame mount package is available. For this package, the CCD is glued to an aluminum nitride (ceramic) substrate. The AlN is narrower than the CCD in the row direction so that the wire bond pads are exposed, and longer in the column direction to facilitate mounting in a window frame style printed circuit board. The PCB has two 37 pin connectors receptacle-type connectors (Airborn NM-122-037-161-JCAC). The pinout is given in Table 5. The CCD is wirebonded to the pads on the inner edges of the cutout. See Figure 14 for the layout of the PCB and its dimensions.

Table 5

Pin Number	J1 Signal	J2 Signal
1	VSUB	VSUB
2	H1(L1)	H1(U2)
3	H2(L1)	H2(U2)
4	H3(L1)	H3(U2)
5	RG(L1)	RG(U2)
6	VR(L1)	VR(U2)
7	VOUT(L1)	VOUT(U2)
8	VDD(L1)	VDD(U2)
9	OG(L1)	OG(U2)
10	SW(L1)	SW(U2)
11	TG(1)	TG(2)
12	P+	P+
13	FS1(1)	FS1(2)
14	FS2(1)	FS2(2)
15	FS3(1)	FS3(2)
16	V1(1)	V1(2)
17	V2(1)	V2(2)
18	V3(1)	V3(2)
19	N+	N+
20	V3(2)	V3(1)
21	V2(2)	V2(1)
22	V1(2)	V1(1)
23	FS3(2)	FS3(1)
24	FS2(2)	FS2(1)
25	FS1(2)	FS1(1)
26	P+	P+
27	TG(2)	TG(1)
28	SW(L2)	SW(U1)
29	OG(L2)	OG(U1)
30	VDD(L2)	VDD(U1)
31	VOUT(L2)	VOUT(U1)
32	VR(L2)	VR(U1)
33	RG(L2)	RG(U1)
34	H3(L2)	H3(U1)
35	H2(L2)	H2(U1)
36	H1(L2)	H1(U1)
37	VSUB	VSUB

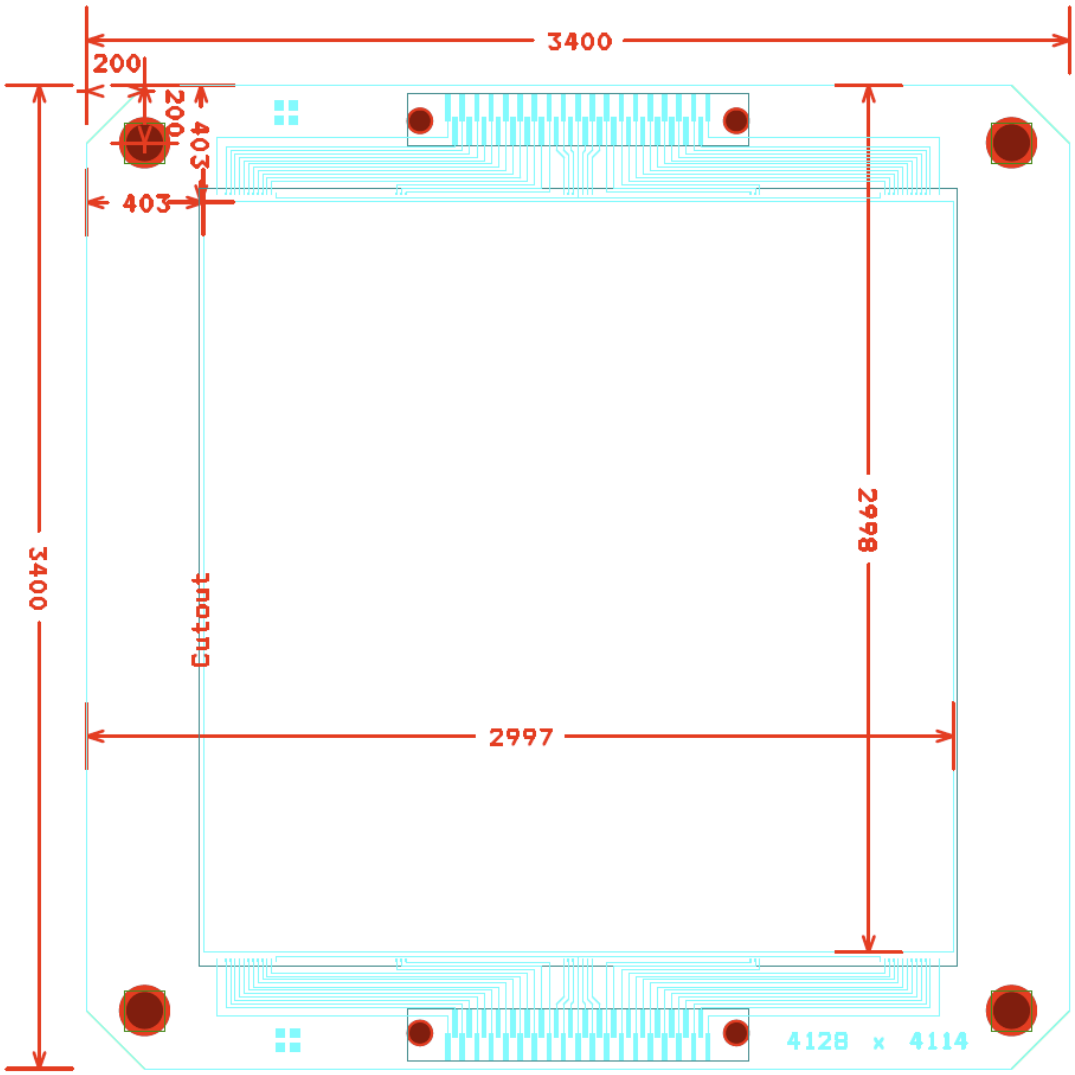


Figure 14 PCB board layout for window frame style package for 4k x 4k format CCD, showing the component side (opposite to the light-sensitive side of the CCD). Dimensions are given in thousandths of an inch. The four corner holes are for mounting and are 0.125” in diameter.

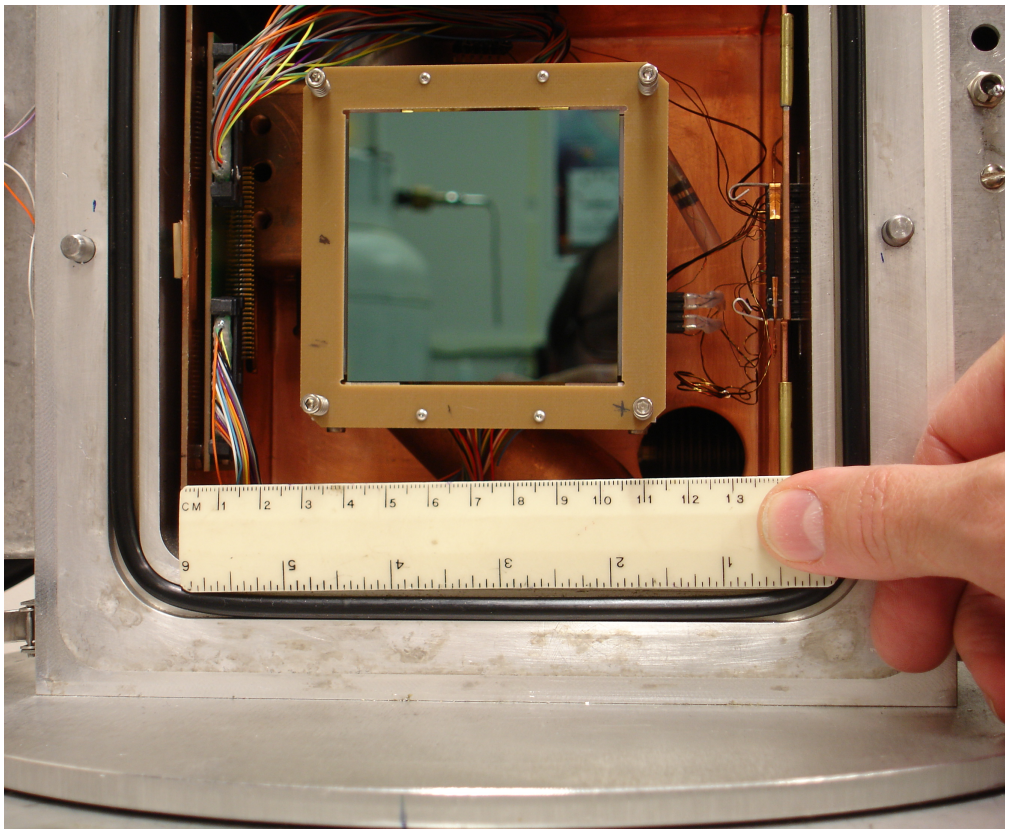


Figure 15 Window-frame packaged 4k x 4k format CCD mounted in the test dewar at LBNL. We use spring loaded cold finger that contacts the AlN substrate on the back; a custom cold plate can also be glued to the AlN substrate by special arrangement.